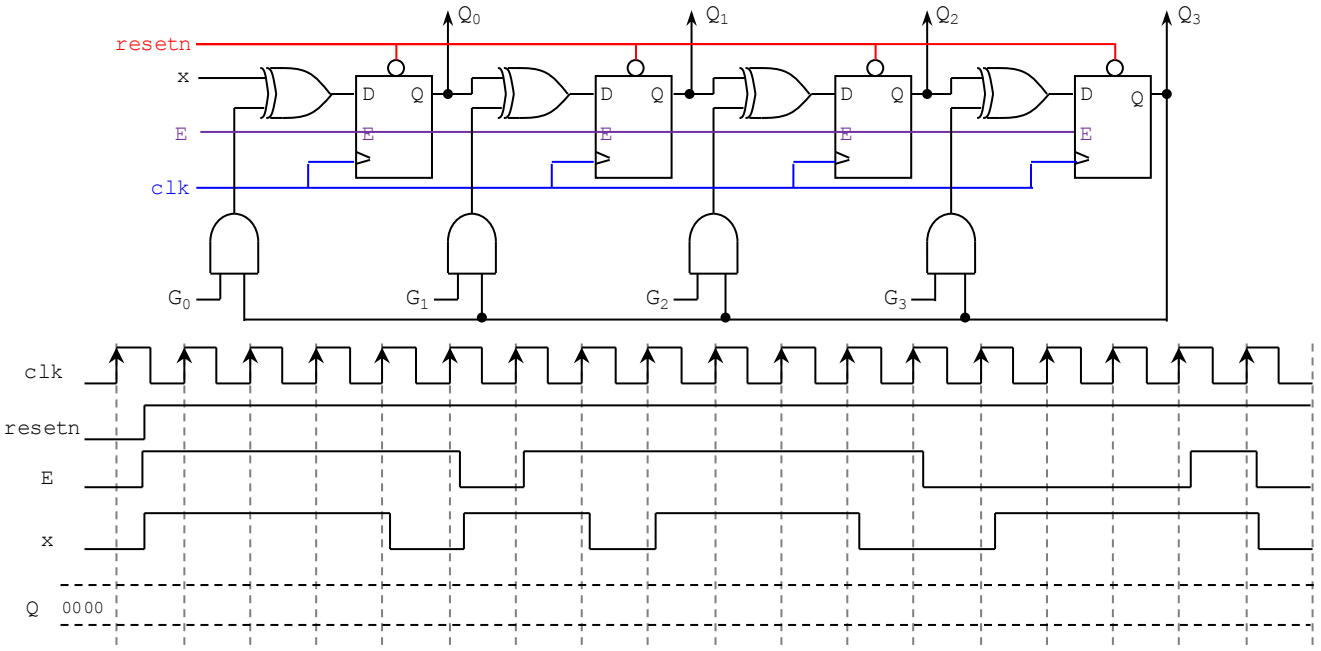
Homework 4

(Due date: April 1st @ 11:59 pm)

Presentation and clarity are very important! Show your procedure!

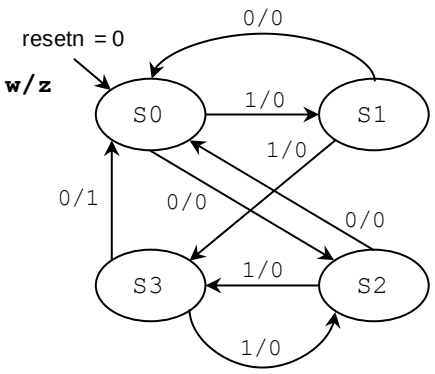
PROBLEM 1 (13 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1101$, $Q = Q_3Q_2Q_1Q_0$

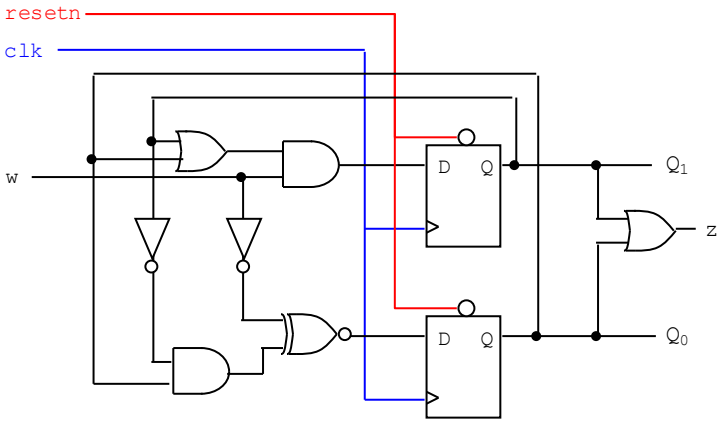


PROBLEM 2 (20 PTS)

- Given the following State Machine Diagram: (10 pts)
  - ✓ Provide the State Table and the Excitation Table. (3 pts)
  - ✓ Get the excitation equations and the Boolean equation for z. (3 pts)
    Use S0 (Q=00), S1 (Q=01), S2 (Q=10), S3 (Q=11) to encode the states.
  - ✓ Sketch the Finite State Machine circuit. (3 pts)
  - ✓ Is it a Mealy or Moore Machine?

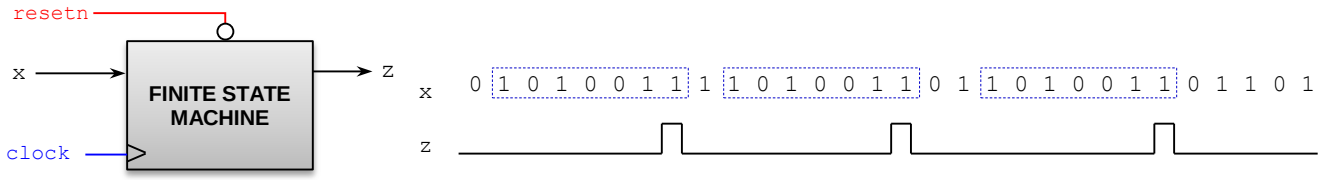


- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following Finite State Machine: (10 pts)



PROBLEM 3 (21 PTS)

- Sequence detector: The machine generates $z = 1$ when it detects the sequence 1010011. Once the sequence is detected, the circuit looks for a new sequence.



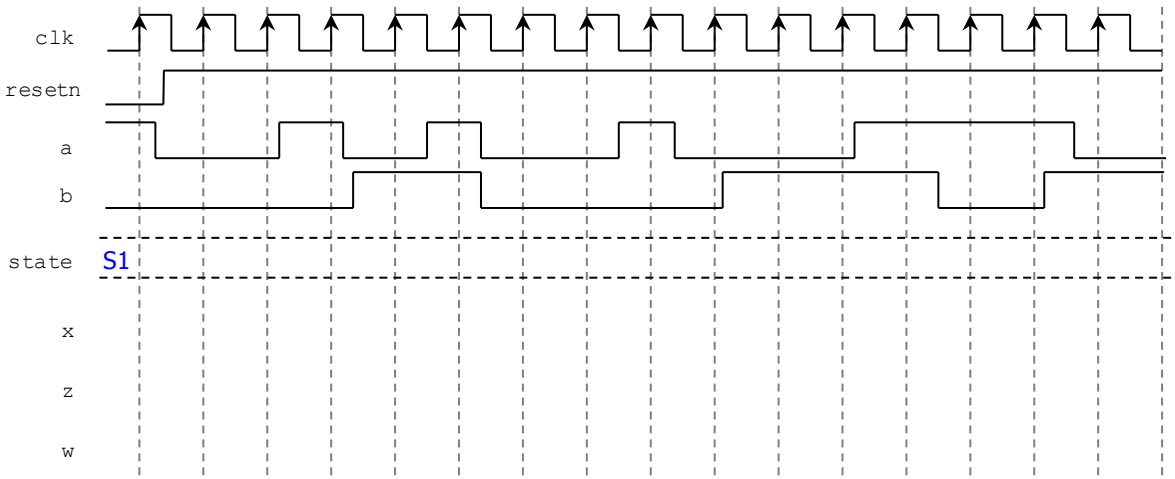
- Draw the State Diagram (any representation), State Table, and the Excitation Table of this circuit with input x and output z. (14 pts)
- Provide the excitation equations and the Boolean equation for z (simplify your circuit: K-maps or Quine-McCluskey).
- Sketch the circuit. Is this a Mealy or a Moore machine? Why? (3 pts)

PROBLEM 4 (14 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description is shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

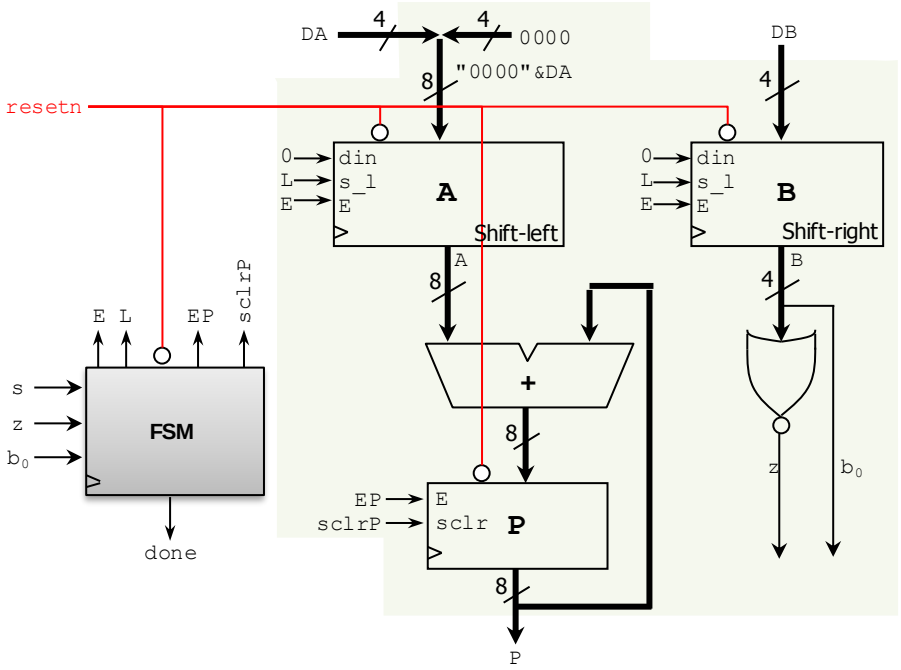
```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, resetn: in std_logic;
          a, b: in std_logic;
          x,w,z: out std_logic);
end circ;
```

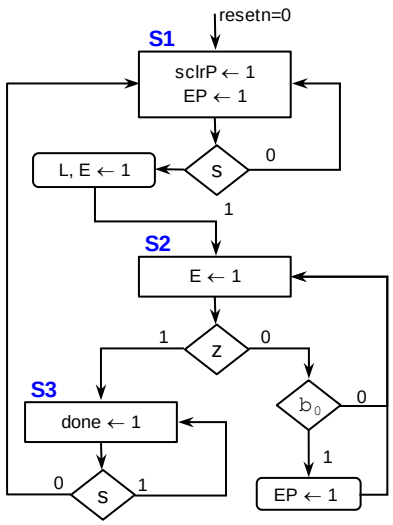
```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, a, b)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if a = '1' then
              if b = '1' then y <= S3; else y <= S1; end if;
            else
              y <= S2;
            end if;

          when S2 =>
            if b = '1' then y <= S3; else y <= S2; end if;

          when S3 =>
            if a = b then y <= S3; else y <= S1; end if;
        end case;
     end if;
  end process;

  Outputs: process (y, a, b)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if a = '1' then x <= '1'; end if;
         when S2 => w <= '1';
         when S3 => if a = b then z <= '1'; end if;
      end case;
  end process;
end behavioral;
```

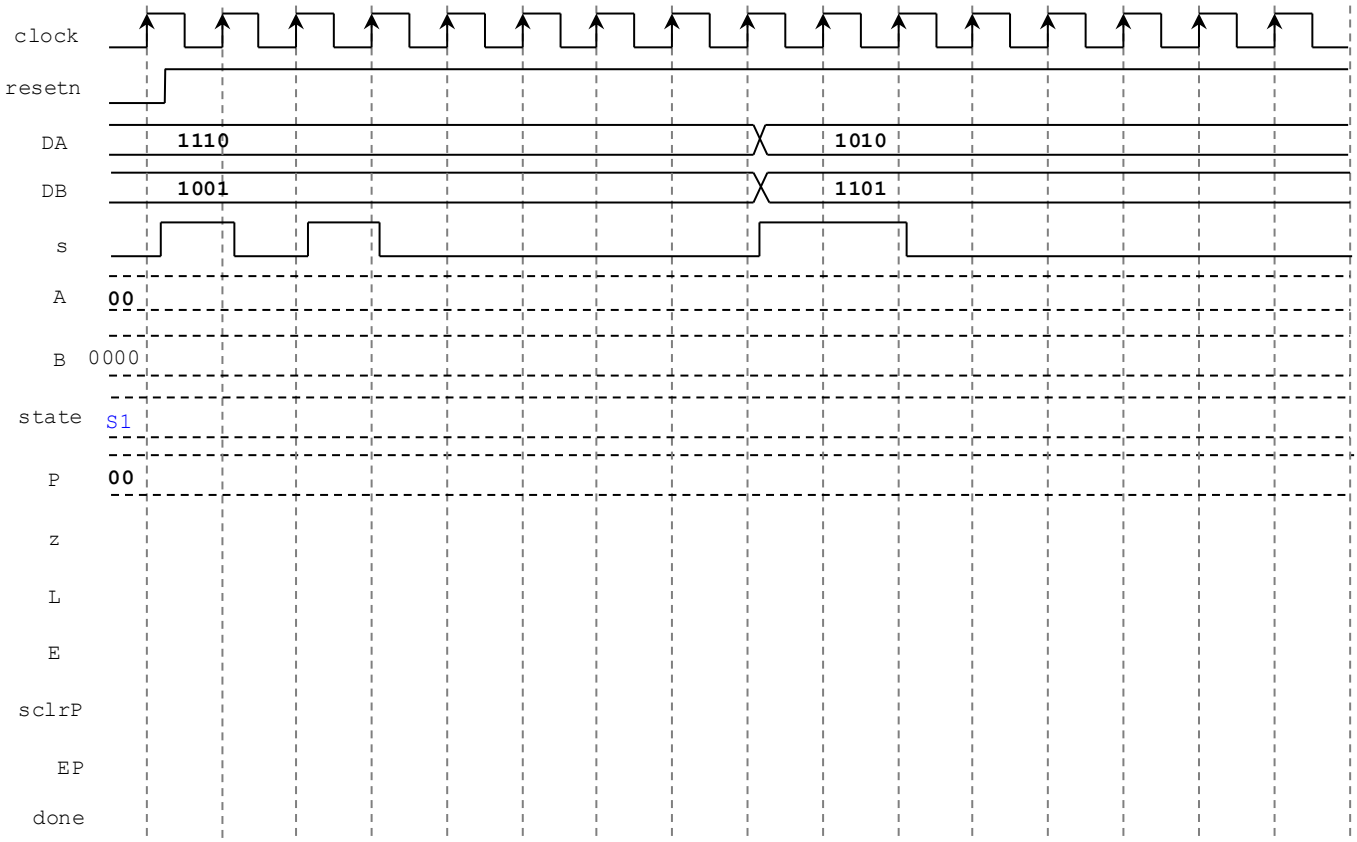


PROBLEM 5 (17 PTS)

- Complete the following timing diagram (`A` and `P` are specified as hexadecimals) of the following Iterative unsigned multiplier. The circuit includes an FSM (in ASM form) and a datapath circuit.
- Refer to the Lecture Notes for more details of the behavior of the generic components:
  - ✓ Register (for `P`): $sclr$: synchronous clear. Here, if $E = sclr = 1$, the register contents are initialized to 0.
  - ✓ Parallel access shift registers (for `A` and `B`): If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift







PROBLEM 6 (15 PTS)

- Attach a printout of your Project Status Report (no more than 3 pages, single-spaced, 2 columns). This report should contain the current status of the project, including more details about the design and its components. You **MUST** use the provided template (`Final Project - Report Template.docx`).